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The block diagram illustrates the internal components of a video camera system. At the top, an antenna (1) is connected to an AGC (Automatic Gain Control) block (2). The AGC block is part of a dashed-line enclosure that also contains a PLL (Phase-Locked Loop) block (3) and an Osc (Oscillator) block (4). The PLL block is connected to a D/A (Digital-to-Analog) converter block (5). The Osc block is connected to a PLL block (6) and an A/D (Analog-to-Digital) converter block (7). The A/D block is connected to a DEMODULATION FEC (Demodulation and Forward Error Correction) block (8). The DEMODULATION FEC block is connected to an AV Dec (Audio/Video Decoder) block (9). The AV Dec block is connected to a D/A block (10) and a D/A block (11). The D/A block (10) is connected to a NOISE SOURCE block (12). The D/A block (11) is connected to a NOISE SOURCE block (13). The NOISE SOURCE block (12) is connected to a summing junction (14). The NOISE SOURCE block (13) is connected to a summing junction (15). The summing junction (14) is connected to an OSD (On-Screen Display) block (16). The summing junction (15) is connected to a D/A block (17). The D/A block (17) is connected to a CPU (Central Processing Unit) block (23). The CPU block (23) is connected to a MEMORY block (24). The CPU block (23) is also connected to a LIGHT RECEIVER block (22). The LIGHT RECEIVER block (22) is connected to a REMOTE CONTROL TRANSMITTER block (25). The REMOTE CONTROL TRANSMITTER block (25) is connected to an antenna (1). The antenna (1) is also connected to the AGC block (2). The antenna (1) is also connected to the PLL block (3). The antenna (1) is also connected to the Osc block (4). The antenna (1) is also connected to the A/D block (7). The antenna (1) is also connected to the DEMODULATION FEC block (8). The antenna (1) is also connected to the AV Dec block (9). The antenna (1) is also connected to the D/A block (10). The antenna (1) is also connected to the D/A block (11). The antenna (1) is also connected to the NOISE SOURCE block (12). The antenna (1) is also connected to the NOISE SOURCE block (13). The antenna (1) is also connected to the summing junction (14). The antenna (1) is also connected to the summing junction (15). The antenna (1) is also connected to the OSD block (16). The antenna (1) is also connected to the D/A block (17). The antenna (1) is also connected to the CPU block (23). The antenna (1) is also connected to the MEMORY block (24). The antenna (1) is also connected to the LIGHT RECEIVER block (22). The antenna (1) is also connected to the REMOTE CONTROL TRANSMITTER block (25).

The graph illustrates the relationship between the receiving level and the frequency of error correction. The vertical axis represents the 'RECEIVING LEVEL' with marked points d, a, a'', b, and c. The horizontal axis represents the 'FREQUENCY OF ERROR CORRECTION' with marked points d', f, a', e, b', and c'. A curve labeled 'NOISE CONTROL VOLTAGE' starts at a low frequency and low receiving level, rising steeply and then leveling off. A curve labeled 'FREQUENCY OF ERROR CORRECTION' starts at a high frequency and high receiving level, falling steeply and then leveling off. The area between these two curves is shaded with diagonal lines and labeled 'ERROR CORRECTABLE RANGE'. Dashed lines connect the points on the curves to their respective values on the axes. For example, at receiving level 'a', the frequency of error correction is 'a'', and the noise control voltage is 'a'.

REPLACEMENT DRAWINGS
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Fig. 3

(a)



(b)



(c)



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